UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/520,107	09/16/2005	Mamoru Kudo	SON-2783	2802

23353 7590 11/12/2008

RADER FISHMAN & GRAUER PLLC
LION BUILDING
1233 20TH STREET N.W., SUITE 501
WASHINGTON, DC 20036

EXAMINER	
PATANKAR, ANEETA V	
ART UNIT	PAPER NUMBER
2627	
MAIL DATE	DELIVERY MODE
11/12/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/520,107	KUDO, MAMORU	
	Examiner	Art Unit	
	Aneeta Patankar	2627	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 August 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 January 2005* is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *1/3/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. **Claims 1-15** are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent Pub. No. 2002/0136137 A1 to *Shishido et al.* in view of U.S. Patent No. 6,049,514 to *Todo*.

As to **claims 1, 4 and 13**, *Shishido* discloses a recording apparatus, method, and medium characterized by comprising: bit pattern determining means which determines a bit pattern of coupling bits to be inserted into predetermined positions of main data encoded by a predetermined recording/encoding format (Fig. 8 and 9, paragraph 0173), where each 16-bit pattern is coupled into coupling bits, and is able to determines said bit pattern of said coupling bits based on sub data to be recorded on a recording medium together with said main data (Fig. 5, paragraph 0177), where the sub code or sub data is in the control signal which controls the data recorded on the medium; coupling bits inserting means and sequence for inserting said coupling bits of said bit pattern determined by said bit pattern determining means and sequence into said predetermined positions of said encoded main data (Fig. 9, paragraph 0176, lines 3-6), where the figure shows the coupling bits inserting means and sequence; and recording means and sequence for recording information formed by inserting said coupling bits

into said main data, on said recording medium (Fig. 8 and 9, paragraph 0173, lines 4-5), where the coupling bits form a data stream that is recorded on the disc, wherein the bit pattern of the coupling bits is selected (Fig. 8 and 9, paragraph 0176, lines 1-6), where two coupling bits are selected, and wherein said coupling bits based on sub data are inserted only at positions which allow an optional selection of at least two bit patterns (Fig. 8 and 9, paragraph 0176, lines 1-6), where at least two coupling bits are required and are inserted at specific positions.

Shishido is deficient in disclosing a digital sum value converges as near to zero as possible.

However *Todo* discloses a digital sum value converges as near to zero as possible (Fig. 1, column 7, lines 12-13), where the digital sum value converges to 0.

At the time of invention, it would have been obvious to a person of ordinary skilled in the art to have modified the recording apparatus comprising bit pattern determination means as taught by *Shishido* by including a digital sum value that converges as near to zero as possible as taught by *Todo*. The suggestion/motivation would have been in order to compensate the dc level of the modulating data by detecting it in advance (Todo, column 7, lines 16-19).

As to **claims 2, 5 and 14**, *Shishido* discloses the recording apparatus, recording method, and recording medium, characterized in that: said bit pattern determining means is configured to carry out the determination of a bit pattern based on said sub data with regard to coupling bits to be inserted between two signal units (Fig. 5, paragraph 0166, lines 2-3), where the signal units handle the bits, both of which have

fixed bit patterns and are' in a forward and backward relation among signal units forming said main data (Fig. 19, paragraph 0241), where the data packets consists of the bit patterns are fixed by the fix-length packet-write method.

As to **claims 3, 6, 9, 12, and 15**, *Shishido* discloses the recording apparatus, method, and medium and reproducing apparatus and method, characterized in that: said two signal units are a frame synchronizing signal and a subcode sync (Fig. 6, paragraph 0177), where the frame synchronizing signal and the control signal which is a subcode, is added to the frame.

As to **claims 7 and 10**, *Shishido* discloses a reproducing apparatus and method, characterized by comprising and executing: reading means and sequence for extracting and reading coupling bits from a recording medium recording information constituted by at least main data encoded by a predetermined recording/encoding format (Fig. 6, 8 and 9, paragraphs 0173 and 0178), where each 16-bit pattern is coupled into coupling bits, and said coupling bits to be inserted only into predetermined positions of said main data which allow an optional selection of at least two bit patterns (Fig. 8 and 9, paragraph 0176, lines 1-6), where at least two coupling bits are required and are inserted at specific positions; and data value acquiring means and sequence for acquiring a data value served as sub data by utilizing a bit pattern of said coupling bits read by said reading sequence and means (Fig. 6, paragraph 0179), where the bits are read from the disc and are output as a stereo audio signal;

Shishido is deficient in disclosing the data value acquiring means performs digital sum value control.

However, *Todo* discloses the data value acquiring means performs digital sum value control (Fig. 2, column 4, lines 29-33), where the modulating data generator (30) controls the digital sum value. In addition, the same motivation is used as the rejection in claim 1.

As to **claims 8 and 11**, *Shishido* discloses the reproducing apparatus and method, characterized in that: said reading means and sequence extracts coupling bits inserted between two signal units (Fig. 5, paragraph 0166, lines 2-3), where the signal units handle the bits, both of which have fixed bit patterns and are in a forward and backward relation among signal units forming said main data (Fig. 19, paragraph 0241), where the data packets which are the bit patterns are fixed by the fix-length packet-write method; and said data value acquiring means and sequence acquires said value data served as sub data based on the combination of either one of bit patterns held by said two signal units (Fig. 5, paragraph 0166, lines 1-3), where the signal units handle the bits, and a bit pattern of said coupling bits (Fig. 8, paragraph 0173, lines 4-5).

Response to Arguments

3. Applicant's arguments filed 8/6/08 have been fully considered but they are not persuasive.

Applicant argues on page 7, lines 13-20 and page 8, lines 10-12, with respect to **claims 1, 4, 7, 10 and 13**, that *Shishido* fails to teach "bit pattern determining means which determines a bit pattern of coupling bits to be inserted into predetermined positions of main data encoded by a predetermined recording/encoding format, and is able to determine said bit pattern of said coupling bits based on sub data to be recorded

on a recording medium together with said main data" and specifically points out that *Shishido* fails to teach "coupling bits between symbols" in these claims.

Examiner disagrees as *Shishido* discloses "bit pattern determining means which determines a bit pattern of coupling bits to be inserted into predetermined positions of main data encoded by a predetermined recording/encoding format" (Fig. 8 and 9, paragraph 0173), where each 16 bit pattern is coupled into coupling bits, "and is able to determine said bit pattern of said coupling bits based on sub data to be recorded on a recording medium together with said main data" (Fig. 5, paragraph 0177), where the sub code or sub data is in the control signal which controls the data recorded on the medium.

Examiner disagrees as *Shishido* discloses "coupling bits between symbols" in paragraph 0176, lines 1-6, where at least two coupling bits are placed between symbols.

Applicant also argues that *Shishido* fails to teach "wherein the bit pattern of the coupling bits is selected such that a digital sum value converges as near to zero as possible" and "wherein said coupling bits based on sub data are inserted only at positions which allow an optional selection of at least two bit patterns".

Examiner agrees that *Shishido* fails to teach "wherein the bit pattern of the coupling bits is selected such that a digital sum value converges as near to zero as possible" and "wherein said coupling bits based on sub data are inserted only at positions which allow an optional selection of at least two bit patterns". However, *Shishido* in view of *Todo* does teach these limitations. *Shishido* teaches "wherein the

bit pattern of the coupling bits is selected" (Fig. 8 and 9, paragraph 0176, lines 1-6), where two coupling bits are selected, and "wherein said coupling bits based on sub data are inserted only at positions which allow an optical selection of at least two bit patterns" (Fig. 8 and 9, paragraph 0176, lines 1-6), where at least two coupling bits are required and are inserted at specific positions. *Todo* discloses "a digital sum value converges as near to zero as possible" (Fig. 1, column 7, lines 12-13), where the digital sum value converges to 0.

Conclusion

4. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aneeta Patankar whose telephone number is (571) 272-

9773. The examiner can normally be reached on Monday-Thursday 8-5, Second Friday, 8-4.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Andrea Wellington can be reached on (571) 272-4483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Andrea L Wellington/
Supervisory Patent Examiner, Art Unit 2627

/A.P./
11/7/08